SIUE **Final Examination Cover Sheet**

Sample MS Degree in Electrical and Computer Engineering

Name: _____

ID Number: _____

Contact information: _____

_____

Indicate the two areas you select:

Subject area 1: _____

Subject area 2: _____

Exam results

Problem	Grade (0–5)	Graded by	Comments

Total score received: _____out of 25 pts. Recommendation: PASS / FAIL (circled).

TABLE OF CONTENTS

Instructions for MS ECE Final Written Examination

This exam is composed of questions in the following subject areas:

1. Communications Systems
2. Computer Design
3. Computer Vision and Image Processing (CVIP)
4. Digital Signal Processing (DSP)
5. IC Design
6. Power and Control Systems

- Choose two subject areas from the list above. The choice of problems is restricted to only two areas. Clearly indicate your selected subject areas by writing them in the appropriate place on the cover sheet.
- Solve 5 problems total. The problems must come from the two selected subject areas. Three from one area and two from the other.
- Do **NOT** work on back of pages, use extra pages if necessary, write the subject area, problem number and your name at the top of each page. Number the pages for your answers, starting with page '1' for each problem.
- You may use: your own textbooks, your own calculator, **NO** internet enabled calculators**, NO** interlibrary loan books, **NO** notes or other papers, **NO** cell phones,
- The exam is **1 hour and 50 minutes**
- After completed, **put only the cover sheet and the five problems you worked clipped together**, put any unused problems, etc, in the second stack of papers

    - Grades will be based only on written evidence in the submitted work.
    - If you work more than five problems only the first five will be graded.
    - Full credit will be given for professional work only: clear, concise, simple, and complete.
    - Always show your work. Answers without sufficient supporting work will be awarded a zero score.
    - If you provide multiple answers to a problem that has a unique solution, only one of your solutions will be picked for grading: top-most or left-most, not necessarily the correct one.
    - Be sure to read the problems carefully, there will be no credit for solutions to misread problems.
    - Measurement units are considered an important part of the answer. Answers given with incorrect units or unit prefixes may be considered wrong even if the numeric part is right.
    - Every problem will be graded on a scale of 0-5 with 5 being the most. A total score of 15 is needed to pass the exam.

ECE Master's Exit Exam **Communications Systems**

#1) A error-correction coding scheme uses 4 transmitted codewords S_1, S_2, S_3, and S_4 as follows:

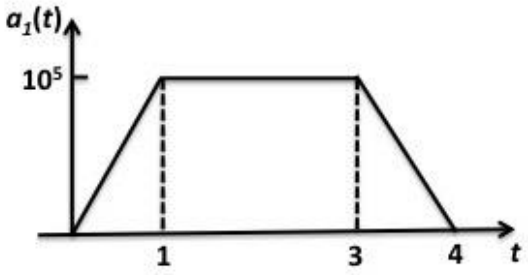
S_1	00000000
S_2	10101010
S_3	11110000
S_4	00001111

(a) Find the number of errors the decoder can detect.

(b) Determine if the code is linear

ECE Master's Exit Exam **Communications Systems**

#2) The signal $a_1(t)$ is shown in the figure, and let $a_2(t) = \sin(2\pi 10^4 t)$



a.) If $a_1(t)$ is frequency modulated by a carrier with frequency 10^6 Hz and D_f = 6 Hz/V, what is the maximum instantaneous frequency of the modulated signal?

b.) If $a_1(t)$ is phase modulated with $D_p = 4\pi$ rad/V, what is the maximum instantaneous frequency of the modulated signal? What is the minimum one?

c.) If $a_2(t)$ is frequency modulated with $D_f = 10^3$ Hz/V, what is the maximum instantaneous frequency of the modulated signal? What is the frequency modulation index?

ECE Master's Exit Exam Communications Systems

#3) An ideal bandpass filter has the following specifications:

Filter gain = 3; Center frequency of the passband = 1 GHz; Filter bandwidth = 2 MHz.
The input to the filter is additive white Gaussian noise (AWGN) with a power spectral density of 10^{-7} w/Hz
Evaluate the average power of the output of the bandpass filter

ECE Master's Exit Exam Computer Design

#1) Before a pipeline is added, the propagation delay through the combinational logic to perform a task was measured as tpd = 240 ns. There is a register before and a register after the combinational logic block. The setup time of a register is 5 ns and the propagation delay through a register is also 5 ns.
a) What is the maximum frequency of the clock for the circuit described above?
b) A 3-segment pipeline is used where the delays through each of the segments are as follows: t1 = 80 ns, t2 = 100 ns, t3 = 60 ns. The registers used in the pipeline are the same as those used above. Sketch the pipelined circuit.
c) What is the maximum frequency of the clock now?
d) What is the speedup factor, S, if 100 tasks are performed?

ECE Master's Exit Exam Computer Design

#2) Explain what is meant by the phrase" microprogrammed control unit." Briefly explain the difference between" horizontal" and" vertical" microcode. What is a nano-memory and a nano-program, and when are their use beneficial?

ECE Master's Exit Exam Computer Design

#3) A finite-state machine has 2^n possible states. At each clock pulse, it reads in a k-bit symbol, emits an m-bit output symbol (including feedback bits), and switches to a new state. The symbol emitted and the new state depends on the current state and the input symbol.
a) Draw a block diagram indicating how the machine can be implemented using a ROM. Explain your diagram.
b) Determine how big the ROM must be. Explain.
c) A non-pipelined processor has a microcode-based controller implemented as a finite-state machine of the sort indicated above. Explain what the states, the k-bit input symbol, and the m-bit output symbol correspond to in this context. How is the instruction processing accomplished?
d) A given processor has an instruction set containing 16 instructions. The average CPI (clocks per instruction) when the cache hit probability is 100%, is 5. Determine the required size of the ROM. Explain how you arrived at your answer, and state any assumptions you have made.

ECE Master's Exit Exam Computer Vision & Image Processing

#1) The HD format for a television display is a 16:9 aspect ratio, where 16 is the horizontal width compared to 9 for the vertical height. Assume the viewer sits six times the picture height from the screen, and the standard spatial cutoff frequency. a) How many pixels per line are needed? b) How many lines are needed in the display?

c) Apply hysteresis thresholding to the following image using 8-connectivity. Use a high threshold of 11 and a low threshold of 5.

$$\begin{bmatrix} 6 & 3 & 3 & 6 & 12 \\ 3 & 6 & 6 & 6 & 4 \\ 4 & 15 & 14 & 0 & 0 \\ 7 & 15 & 0 & 0 & 0 \\ 0 & 7 & 3 & 1 & 0 \end{bmatrix}$$

ECE Master's Exit Exam Computer Vision & Image Processing

#2) For the following 2-bit-per-pixel image, a) find the gray level co-occurrence matrix for the vertical direction (90 and 270 degrees), with d = 1, b) Find the gray level co-occurrence matrix for the horizontal direction (0 and 180 degrees), with d = 1, and c) normalize these values.

$$\begin{bmatrix} 1 & 1 & 0 & 0 \\ 2 & 3 & 2 & 3 \\ 1 & 2 & 3 & 3 \\ 3 & 3 & 3 & 0 \end{bmatrix}$$

ECE Master's Exit Exam Computer Vision & Image Processing

#3). An imaging system has a lens with a diameter of 50mm and a focal length of 10mm. The system is setup so that objects at a distance of 3.0 meters are correctly focused. Assume that the imaging device is a CCD with round pixel elements that have a 0.1mm diameter. Describe how an object at a distance of 2.0 meters appears in the image. a) Provide a numeric value to describe the object's image, b) use words to explain how it will appear.

The following two images resulted from transform-domain filtering; the same filter was used with two different transforms. *Note: a post-processing histogram stretch was performed so you can see the image details.* c) Under the image write the name of the transform that that was used. d) Was the filter a highpass or lowpass? e) Was it an ideal or Butterworth filter? f) The image is 256×256. What cutoff frequency was used for the filter? Explain.

ECE Master's Exit Exam Digital Signal Processing

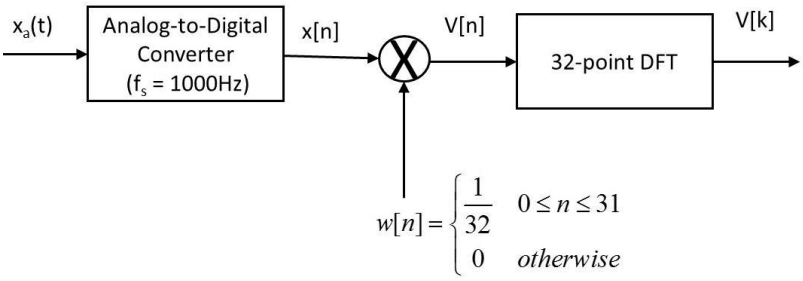
#1) A causal, linear, time-invariant, discrete-time system H with input x_n and output y_n is described by the difference equation:

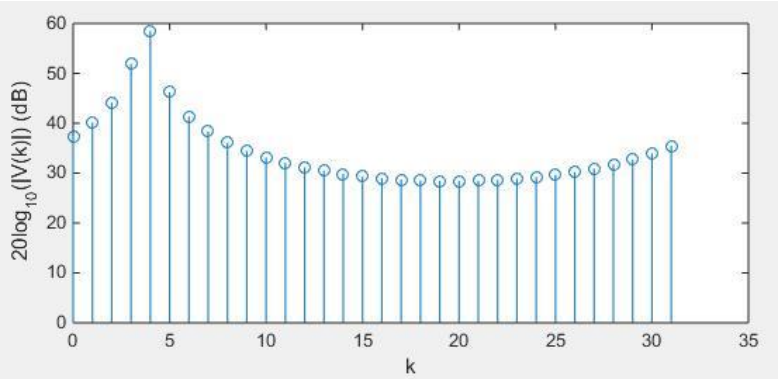
$$Y_n = (5/6)y_{n-1} - (1/6)\, y_{n-2} + x_n - x_{n-2}$$

a) Determine the transfer function $H(z)$ for this system.
b) Sketch the pole-zero diagram for this system.
c) Sketch the magnitude of the frequency response $|H(e^{jw})|$, for $0 < w < \pi$
d) Determine the output sequence y_n for $n = 0,\ldots,10$ using the input sequence x_n: $\{1,1,1\}$. Assume no initial conditions.

ECE Master's Exit Exam Digital Signal Processing

#2) A system for discrete-time spectral analysis of continuous-time signals is shown below. In addition, the output $V[k]$ from the system is shown in the plot. (Note the plot of $V[k]$ is in dB.) One of the ten signals listed below is $x_a(t)$, which is the input to the system shown and produces $V[k]$ as the output. Which signal(s) could be the input to the system? **Important: please provide reasoning and explanation for your answer(s).**





$$x_1(t) = 1000\cos(230\pi t)$$
$$x_2(t) = 1000\cos(115\pi t)$$
$$x_3(t) = 10e^{j(460\pi t)}$$
$$x_4(t) = 1000e^{j(230\pi t)}$$
$$x_5(t) = 10e^{j(230\pi t)}$$
$$x_6(t) = 1000e^{j(250\pi t)}$$
$$x_7(t) = 10\cos(250\pi t)$$
$$x_8(t) = 1000\cos(218.75\pi t)$$
$$x_9(t) = 10e^{j(200\pi t)}$$
$$x_{10}(t) = 1000e^{j(187.5\pi t)}$$

ECE Master's Exit Exam Digital Signal Processing

#3) Give a clear but brief (1 to 3 sentence) answer to each of the following 10 questions.

1. What is the relationship, if any, between the discrete Fourier transform (DFT) and a fast Fourier transform (FFT)?
2. What is the relationship between a discrete-time, linear system that is causal and the unit circle in the complex z-plane associated with the Z-transform of its unit-sample response?
3. Describe the region of convergence of the Z-transform of the unit-sample response of a discrete-time, linear system that is stable.
4. What does it mean to design a discrete-time filter to correspond to a continuous-time filter when the principle of "impulse-invariance" is used?
5. What is the Nyquist condition?
6. Describe the input-output characteristic of an ideal b-bit uniform quantizer.
7. What is Gibbs' overshoot?
8. What is the definition of a linear system?
9. What is aliasing?
10. What is a Butterworth filter of order n?

ECE Master's Exit Exam IC Design

#1) Increasing the width-to-length ratio of a FET will reduce the timing resistance of the FET. One might incorrectly assume that this will always reduce propagation delay.

Explain under what set of circumstances this is true and under what conditions increasing the width to length ratio is likely to do little to improve performance.

ECE Master's Exit Exam **IC Design**

#2) Realize the following function using a fully complementary CMOS complex gate:

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F = (A & B) | (C & D)
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where & is the logical AND operator and | is the logical OR operator.

ECE Master's Exit Exam **IC Design**

#3) Determine device for the FETs described below. Use the agreed upon process parameters.

V_{dd} = 2.5 Volts

$V_{ds,vsat}$ = saturation voltage due to velocity saturation = 0.65 volts for NFETs and -3 volts for PFETs. (Assumes L = 0.25 μm)

Length of all FETS is 0.25 μm.

Threshold voltage of NFET is +0.5 Volts.
Threshold voltage of PFET is -0.5 Volts.

Transconductance parameter of NFET, K_{PN}, is 230 $\mu A/V^2$
Transconductance parameter of PFET, K_{PP}, is 50 $\mu A/V^2$

Neglect both channel length and bulk modulation effects i.e. $\gamma = 0$ and $\lambda = 0$. Assume in each case the width of the FET is 1 μm.

a) What is I_{ds} for a NFET whose gate voltage is 0.25 Volts, drain voltage is 0.1 volts, and source voltage is 0 volts?

b) What is I_{SD} for a PFET whose gate voltage is 0 Volts, source voltage is 2.5 volts, and drain voltage is 1.5 volts?

ECE Master's Exit Exam Power and Control Systems

#1) A three-phase load is connected to a transformer via a feeder. Given the following information to the system and selecting the base values of S_b = 10 MVA and V_b = 10 kV at the load site,
* Transformer: three-phase, 15MVA, 138KV/13.8KV (line voltages), z = j0.04 p.u
* Feeder: 0.5 + j0.5 Ohms
* Load: It consumes 12 MVA at a lagging power factor of 0.7 when the line voltage across its terminals is 13KV

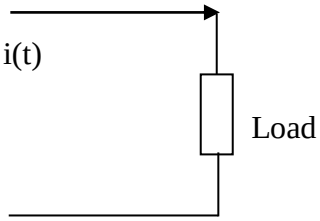
a) compute the base values for two zones: one at the primary side and the other at the secondary side of the transformer.

	primary side of transformer	**secondary side of transformer**
V_b		
I_b		
Z_b		

b) convert all given data in p.u. and draw one line electric diagram
c) find the primary voltage of transformer in p.u. and in kV
d) find the regulation of the system

ECE Master's Exit Exam Power and Control Systems

#2) A monophase load is consuming 25 KVA at a lagging power factor of 0.8 when 200 V is applied (f = 60Hz).



a) Find the current i(t) .

b) Find the shunt (parallel) capacitor bank (in KVAR) to increase its power factor to 0.95 lagging.

c) Assuming that the shunt capacitor bank is available in multiple of 1 KVAR, what is the size of shunt capacitor (in KVAR) to be installed? Also, find the new power factor after installing this capacitor bank.

ECE Master's Exit Exam **Power and Control Systems**

#3) Given a LTI system described by the following differential equations:

$$\dot{x}(t) = \begin{bmatrix} -1 & 1 \\ 1 & -2 \end{bmatrix} x(t) + \begin{bmatrix} 1 \\ 1 \end{bmatrix} u(t)$$
$$y(t) = \begin{bmatrix} 1 & 0 \end{bmatrix} x(t) + u(t)$$

a. Is this system controllable? Is this system observable? Why?
b. Design a state feedback controller $u = -K x$, such that the closed-loop poles are at $-5, -5$.
c. Design a full-order observer matrix K_e such that the desired observer poles at -5, -5.